

## CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

- 1 1. A vertical field effect transistor including  
 2 a semiconductor pillar conduction channel,  
 3 gate electrodes in trenches adjacent said  
 4 semiconductor pillar,  
 5 a layer of insulator adjacent said gate  
 6 electrodes and opposite said semiconductor pillar,  
 7 sidewalls adjacent said semiconductor pillar  
 8 above said gate electrodes in said trenches,  
 9 insulator material in said trenches above said  
 10 gate electrodes and adjacent said sidewalls, [said  
 11 insulator material being selectively etchable  
 12 relative to said sidewalls and said semiconductor  
 13 pillar].
- 1 2. A vertical transistor as recited in claim 1,  
 2 further including isolation material adjacent said  
 3 layer of <sup>insulator</sup> [insulating material] and surrounding said  
 4 vertical transistor, said isolation material [being  
 5 selectively etchable relative to said layer of  
 6 insulator].

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fig. 24C

1 3. A vertical transistor as recited in claim 2,  
2 further including

3 a contact formed in an opening in said  
4 isolation material adjacent [said <sup>insulator material</sup> insulating material]  
5 to [a conductive region at an end of said pillar].

1 4. A vertical transistor as recited in claim 1,  
2 further including

3 *fig. 24C* a contact formed in an opening to an end of  
4 said pillar, and

5 *fig. 23C* a contact formed in an opening adjacent to and  
6 extending above said pillar to said gate structure  
7 and insulated from said pillar by an insulating  
8 sidewall on said pillar.

1 5. A vertical transistor as recited in claim 1,  
2 further including

3 a spacer in said trench between said gate  
4 structure and a bottom of said trench.

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1 6. An integrated circuit device including  
2 isolation material surrounding transistor  
3 locations in a substrate,  
4 vertical field effect transistors formed at  
5 said transistor locations and having a gate  
6 electrode structure formed in a trench,  
7 a layer of insulator material in [said trenches]  
8 between said isolation material and said gate  
9 electrode structure, [said isolation material being  
10 selectively etchable relative to said layer of  
11 insulator] and  
12 a contact opening formed along an interface of  
13 said layer of insulator material and said isolation  
14 material.

figs. 24C,  
38C

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1 7. A device as recited in claim 6, wherein said  
2 gate structure includes dual gate electrodes  
3 extending on opposite sides of a conduction channel.

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1 8. A device as recited in claim 6, further  
2 including  
3 a contact formed in said contact opening in  
4 said isolation material adjacent said [insulating] insulator  
5 material and extending to a conductive region  
6 extending below said pillar.

1 9. A device as recited in claim 6, further  
 2 including  
 3 *fig. 24C* a contact formed in an opening to an end of  
 4 said pillar, and  
 5 *fig. 23C* a contact formed in an opening adjacent to and  
 6 extending above said pillar to said gate structure  
 7 and insulated from said pillar by an insulating  
 8 sidewall on said pillar.

1 10. A device as recited in claim <sup>6</sup>[61], further  
 2 including

3 a spacer in said trench between said gate  
 4 structure and a bottom of said trench.

1 11. A method of making a semiconductor device  
 2 including a field effect transistor, said method  
 3 including steps of  
 4 forming a semiconductor pillar in a trench in a  
 5 body of a first insulating material, said trench  
 6 extending to a layer of semiconductor material,  
 7 forming a layer of a second insulating material  
 8 on walls of said trench, and  
 9 etching a contact opening to said semiconductor  
 10 material through said first insulating material  
 11 selectively and adjacent to said second insulating  
 12 material.

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1 12. A method as recited in claim 11, including  
2 further steps of  
3 forming a gate structure adjacent sides of said  
4 pillar,  
5 forming layers and/or sidewalls of selectively  
6 etchable materials over said gate structure and said  
7 pillar, and  
8 forming contact openings to an end of said  
9 pillar and said gate structure by selective etching  
10 of said layers at locations above and adjacent said  
11 pillar, respectively.

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1 13. A method as recited in claim 11, including  
2 further steps of  
3 defining a height of said pillar by thickness  
4 of a layer of sacrificial material.

1 14. A method as recited in claim 13, wherein said  
2 sacrificial material is germanium oxide.

1 15. A method as recited in claim 11, wherein said  
2 step of forming said pillar is performed by  
3 epitaxial semiconductor growth in a trench.

1 16. A method as recited in claim 11, wherein said  
2 step of forming said pillar is performed by etching  
3 of a layer of semiconductor material.

1 17. A method as recited in claim 11, including a  
 2 further step of  
 3 limiting a dimension of said pillar by a  
 4 distance between isolation structures.

1 18. A transistor comprising  
 2 a substrate,  
 3 a first diffusion,  
 4 a second diffusion above said first diffusion,  
 5 a channel extending vertically between said  
 6 first diffusion and said second diffusion,  
 7 a gate structure extending on at least one side  
 8 of said channel, and  
 9 a contact to said first diffusion borderless to  
 10 said gate structure.

1 19. A transistor as recited in claim 18, wherein  
 2 said transistor is a vertical transistor and wherein  
 3 said first diffusion is formed in said substrate and  
 4 said second diffusion is formed on the channel.

1 ~~20. A transistor as recited in claim 18, wherein~~  
 2 ~~said gate extends on two sides of said channel.~~

1 21. A transistor as recited in claim 19, wherein a  
 2 contact to said gate extends above and on two sides  
 3 of said second diffusion.

fig. 23  
p. 14

1 22. A transistor as recited in claim 19, further  
2 including separate contacts to separate portions of  
3 said gate structure on different sides of said  
4 channel.

1 23. A transistor as recited in claim 18, wherein  
2 said gate structure extends on at least three sides  
3 of said channel.

1 24. A transistor as recited in claim 18, further  
2 including a contact to said second diffusion  
3 borderless to said gate structure.

1 25. A transistor as recited in claim 18, wherein  
2 said transistor comprises a pillar of single crystal  
3 silicon having an edge.

1 26. A transistor as recited in claim 25, wherein  
2 said pillar comprises said first diffusion, said  
3 channel and said second diffusion, said gate  
4 structure extending adjacent said pillar.

1 27. A transistor as recited in claim 26, wherein  
2 said first diffusion extends into single crystal  
3 silicon beneath said pillar and extends below said  
4 gate structure for formation of a contact adjacent  
5 said gate structure.

1 28. A transistor as recited in claim 26, further  
2 comprising  
3 an insulator adjacent said gate structure,  
4 wherein said contact to said first diffusion  
5 comprises a conductive layer adjacent said  
6 insulator.

1 29. A transistor as recited in claim 26, wherein  
2 said gate structure is borderless to said second  
3 diffusion.

1 30. A transistor as recited in claim 26, wherein  
2 said contact to said second diffusion comprises a  
3 spacer self-aligned to said edge.

1 31. A transistor as recited in claim 26, wherein  
2 said pillar extends above said gate structure.

1 32. A transistor as recited in claim 18, further  
2 comprising  
3 an isolation structure, wherein said transistor  
4 is self-aligned to said isolation structure.

1 33. A transistor as recited in claim 18, further  
2 comprising  
3 a contact between said first diffusion and  
4 another diffusion forming part of a second  
5 transistor, wherein said contact between said first  
6 diffusion and said another diffusion extends over  
7 insulation between said first transistor and said  
8 second transistor.

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fig. 39



1 34. A transistor as recited in claim 33, wherein  
 2 said insulation comprises an etched and deposited  
 3 isolation structure.

1 *hde* 35. A transistor as recited in claim 32 wherein  
 2 *97* said substrate comprises SOI having buried oxide  
 3 isolation and wherein said insulation comprises said  
 4 buried oxide isolation.

1 36. A transistor as recited in claim 33, wherein  
 2 said first transistor and said second transistor  
 3 comprise an inverter and wherein said contact to  
 4 said first diffusion is a contact to said inverter.

1 37. A transistor as recited in claim 18, wherein  
 2 said gate structure comprises a continuous interior  
 3 wall entirely surrounding said channel and spaced  
 4 therefrom by a dielectric layer.

1 38. A transistor as recited in claim 18 wherein  
 2 said gate structure is self-aligned to said channel.

1 39. A transistor as recited in claim 18 wherein  
 2 said first diffusion comprises a dopant species  
 3 provided separately from said second diffusion.

1 40. A transistor as recited in claim 18, wherein  
 2 said channel is of sub-lithographic width.

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1 41. A transistor as recited in claim 18, wherein  
 2 said first diffusion includes  
 3 top and side surfaces covered by a dielectric  
 4 material,  
 5 a borderless opening at least through a portion  
 6 of the dielectric material on said top surface, and  
 7 a first diffusion contact formed in the  
 8 opening.

1 42. A transistor as recited in claim 18, wherein  
 2 said second diffusion includes  
 3 top and side surfaces covered by a dielectric  
 4 material,  
 5 a borderless opening at least through a portion  
 6 of the dielectric material on said top surface, and  
 7 a second diffusion contact formed in the  
 8 opening.

1 43. A transistor as recited in claim 18, wherein  
 2 said gate structure includes  
 3 top, bottom and side surfaces covered by a  
 4 dielectric material,  
 5 a borderless opening at least through a portion  
 6 of the dielectric material on said top surface, and  
 7 a gate contact formed in the opening.

1 44. A transistor as recited in claim 18, wherein  
 2 said first diffusion, said second diffusion and said  
 3 gate structure each include a borderless contact.